Al Mansoura University

Faculty of Engineering

Electronics and Communications Dept.

2nd Year Students

Logic Circuit 2

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Chapter 1: Latches

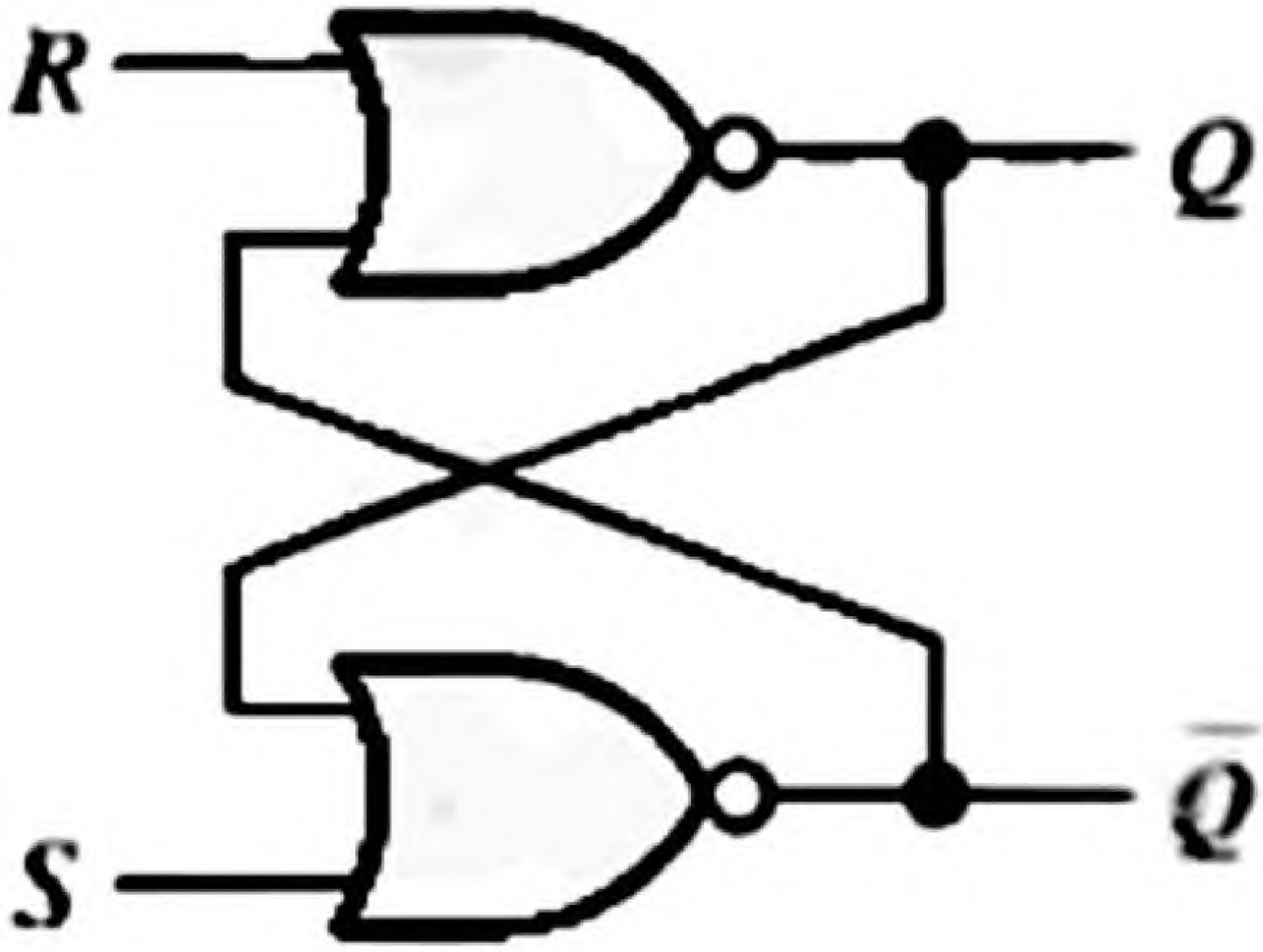
Lecture No. 1

1.1-Latches.

- ✓ The latch is a type of temporary storage device that has two stable states (bistable) and is normally placed in a category separate from that of flip-flops.
- ✓ Latches are similar to flip-flops because they are bistable devices that can reside in either of two states using a feedback arrangement, in which the outputs are connected back to the opposite inputs.
- ✓ The main difference between latches and flip-flops is in the method used for changing their state.

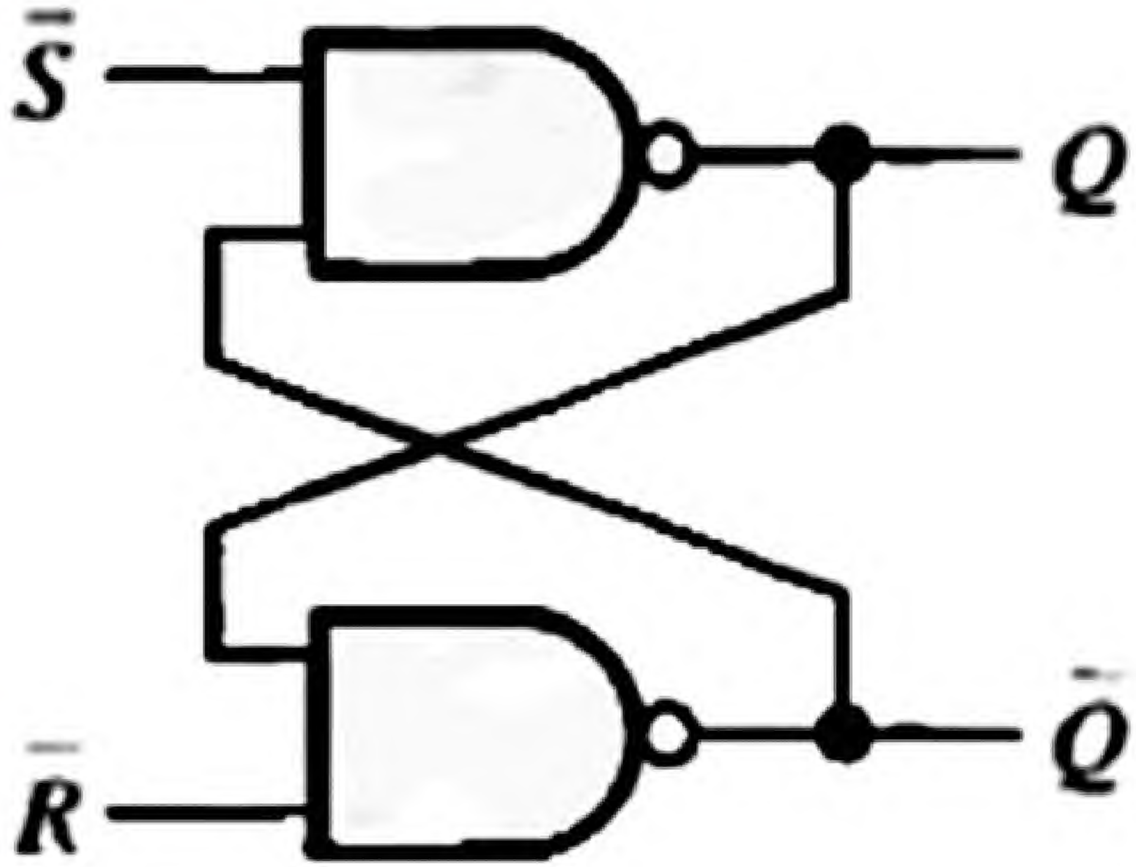
1.2- The S-R (SET-RESET) Latch:

- ✓ A latch is a type of bistable logic device or multivibrator.
- ✓ An active-HIGH input S-R (SET- RESET) latch is formed with two cross-coupled NOR gates, as shown in Figure 1.1(a).



(a) Active-HIGH input S-R latch

- ✓ **An active-LOW input S-R latch is formed with two cross-coupled NAND gates, as shown in Figure 1.1 (b).**



(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

- ✓ Notice that the output of each gate is connected to an input of the opposite gate.
- ✓ This produces the regenerative feedback that is characteristic of all latches and flip-flops.
- ✓ To explain the operation of the latch, we will use the NAND gate S-R latch in Figure 1.1 (b).
- ✓ This latch is redrawn in Figure 1.2 with the negative-OR equivalent symbols used for the NAND gates.

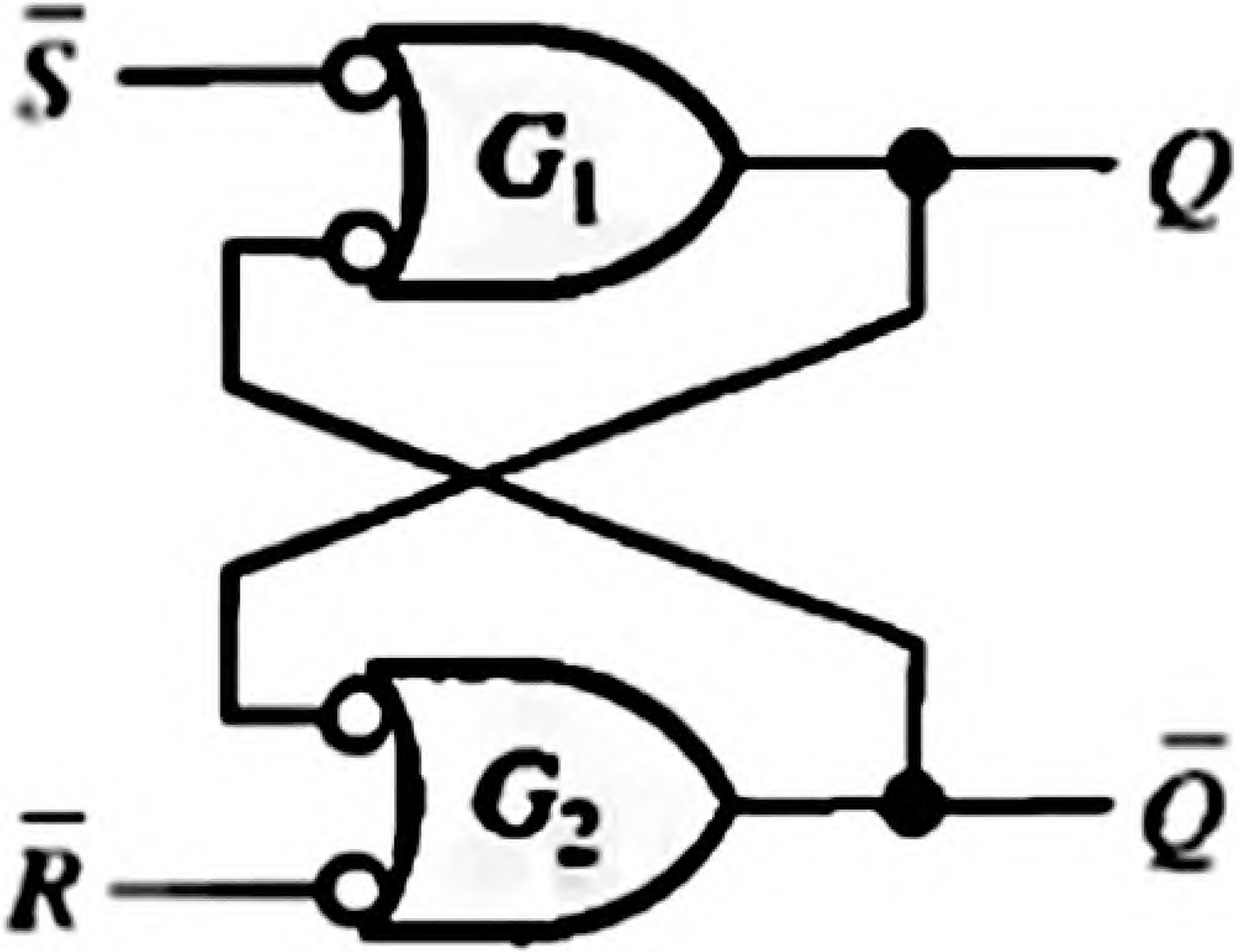
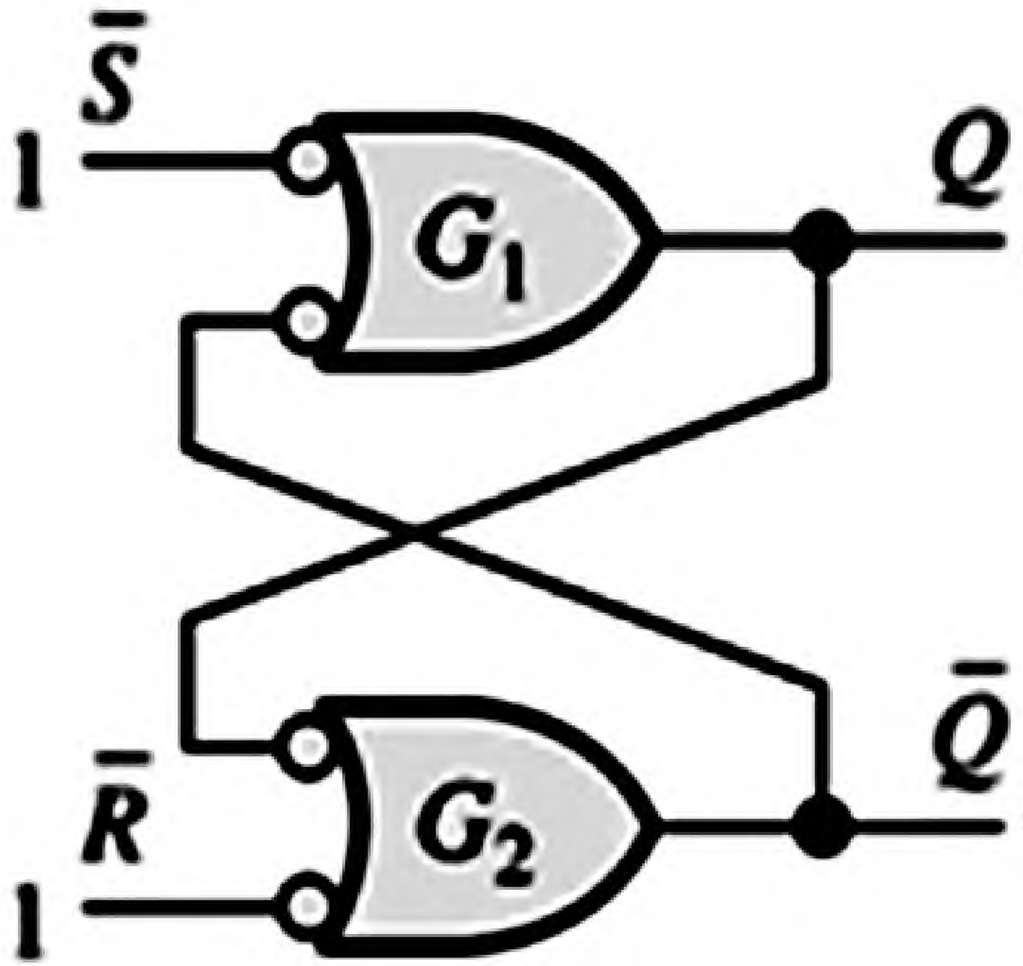


Figure (1.2)

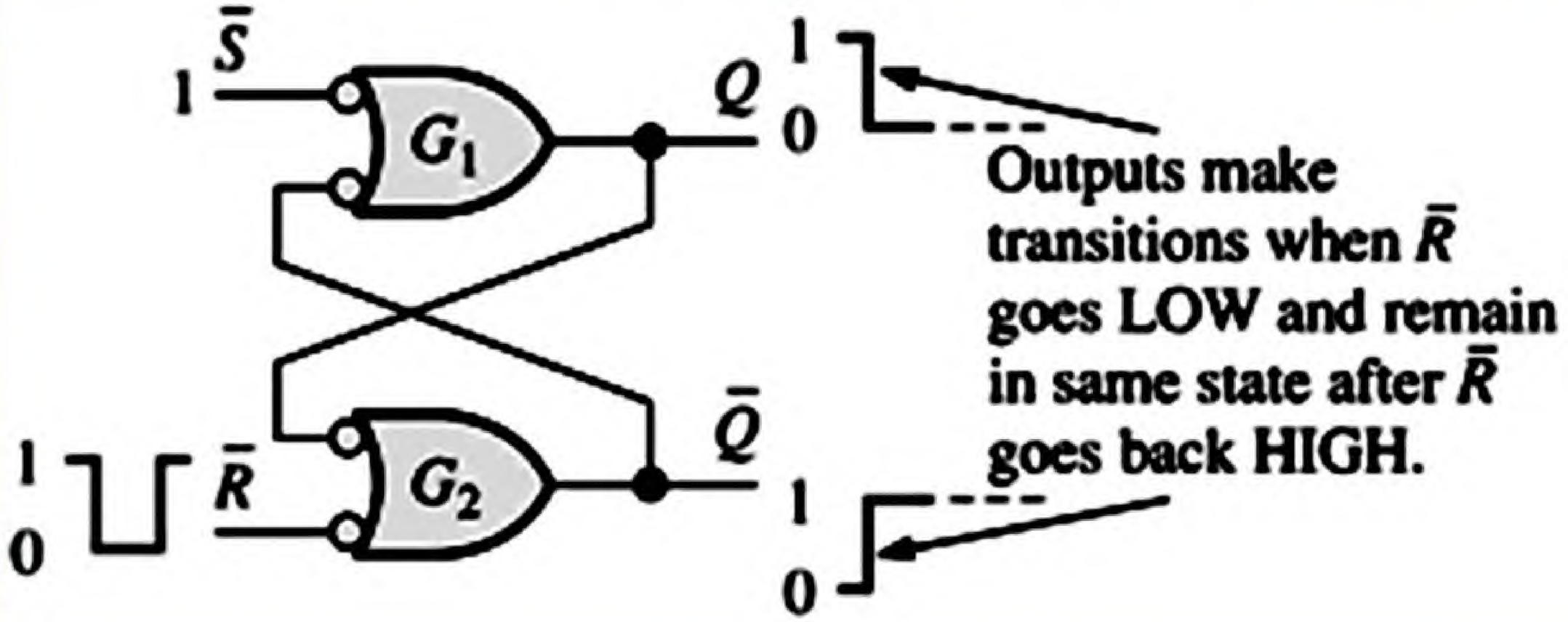
- ✓ **This is done because LOWs on the $\overline{S}$ and $\overline{R}$ lines are the activating inputs.**
- ✓ **The latch in Figure 1-2 has two inputs, $\overline{S}$ and $\overline{R}$, and two outputs, Q and $\overline{Q}$.**
- ✓ **Let's start by assuming that both inputs and the Q output are HIGH as shown in Figure (1.3).**



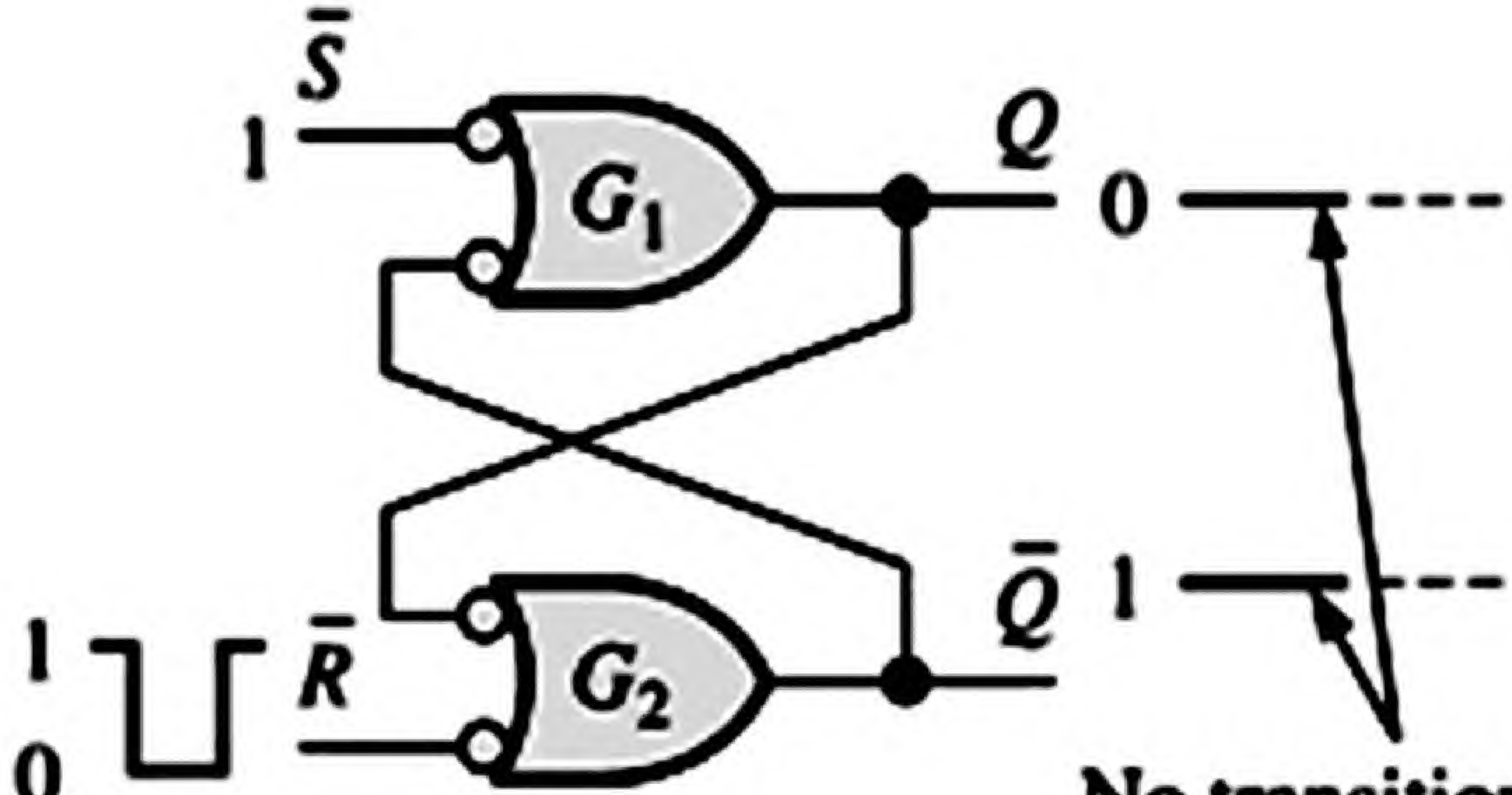
Outputs do not change state. Latch remains SET if previously SET and remains RESET if previously RESET.

HIGHS on both inputs

- ✓ Since the Q output is connected back to an input of gate G_2, and the $\overline{R}$ input is HIGH, the output of G_2, $\overline{Q}$ must be LOW.
- ✓ This LOW output is coupled back to an input of gate G_1 ensuring that its output is HIGH.
- ✓ When the Q output is HIGH, the latch is in the SET state.
- ✓ It will remain in this state indefinitely until LOW is temporarily applied to the $\overline{R}$ input.
- ✓ With a LOW on the $\overline{R}$ input and a HIGH on $\overline{S}$, the output of gate G_2 is forced HIGH.


$\bar{S}$
1
G_1
Q
1
0
Outputs make transitions when $\bar{R}$ goes LOW and remain in same state after $\bar{R}$ goes back HIGH.
$\bar{Q}$
$\bar{R}$
G_2
1
0
1
0

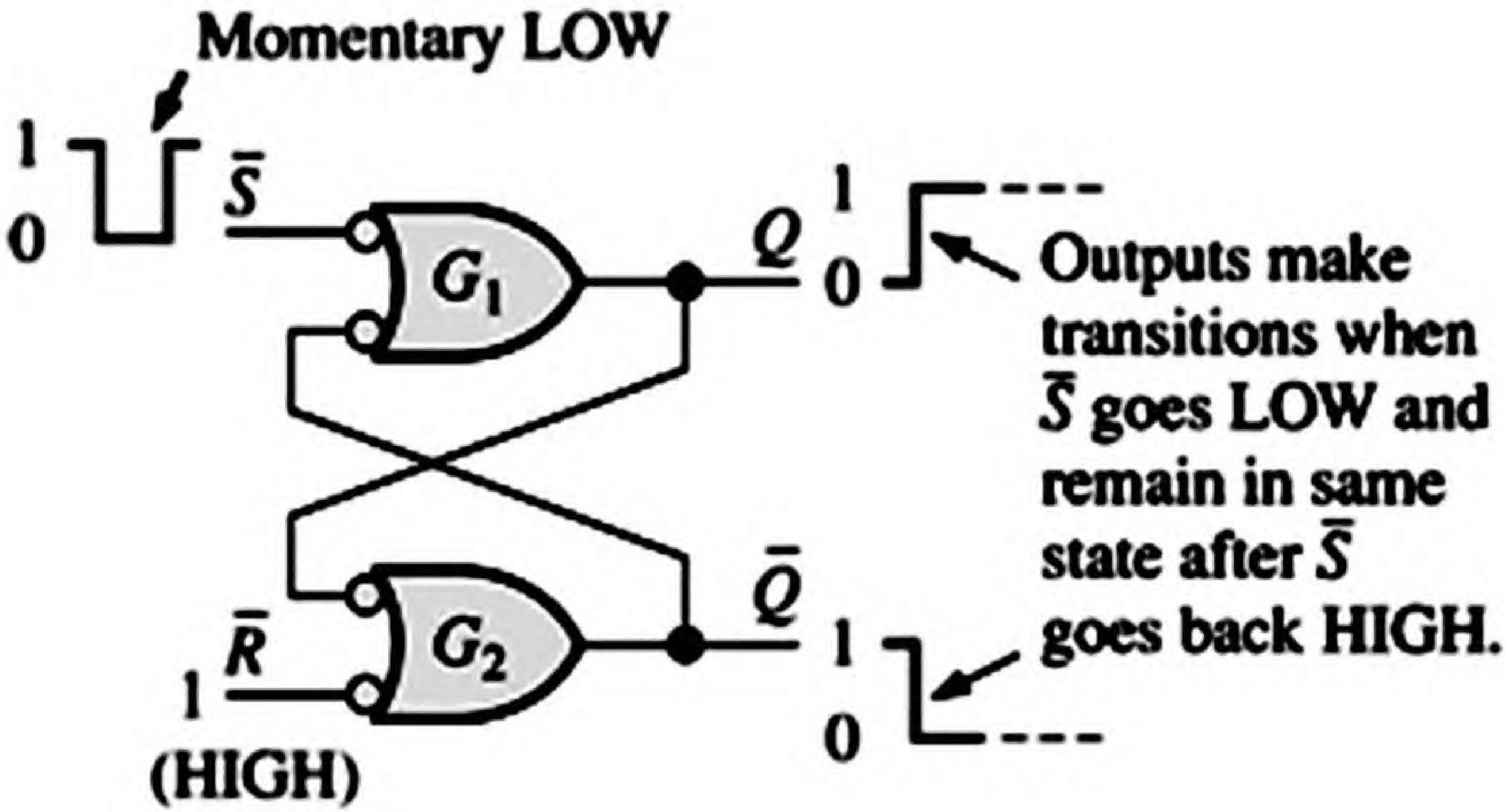
- ✓ **This HIGH on the $\overline{Q}$ output is coupled back to an input of G_1, and since the S input is HIGH, the output of G_1 goes LOW.**
- ✓ **This LOW on the Q output is then coupled back to an input of G_2, ensuring that the $\overline{Q}$ output remains HIGH even when the LOW on the $\overline{R}$ input is removed.**



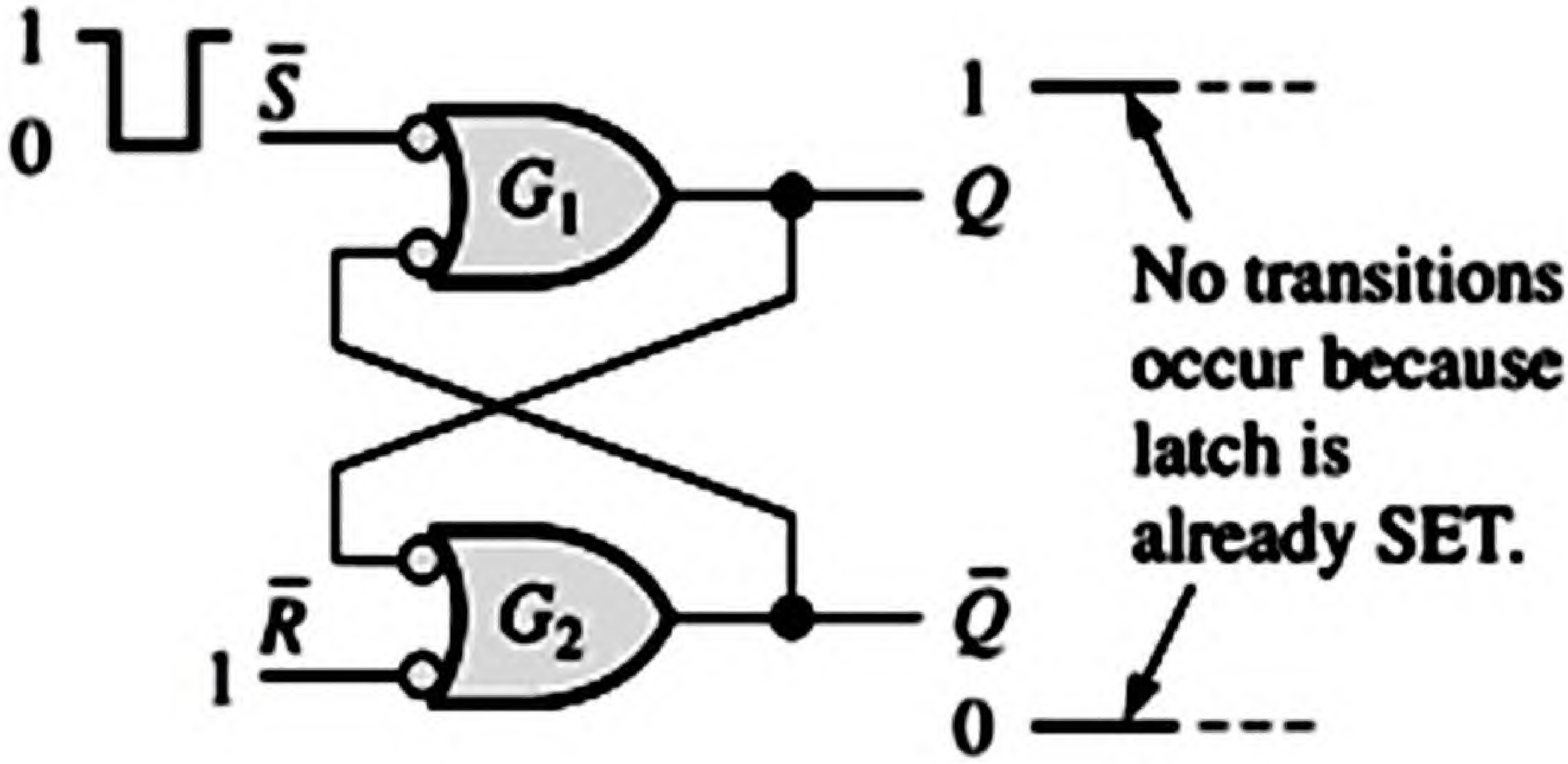
No transitions occur because latch is already RESET.

Latch starts out RESET ($Q = 0$).

- ✓ When the Q output is LOW, the latch is in the RESET state.
- ✓ Now the latch remains indefinitely in the RESET state until a LOW is applied to the S input.
- ✓ In normal operation, the outputs of a latch are always complements of each other.

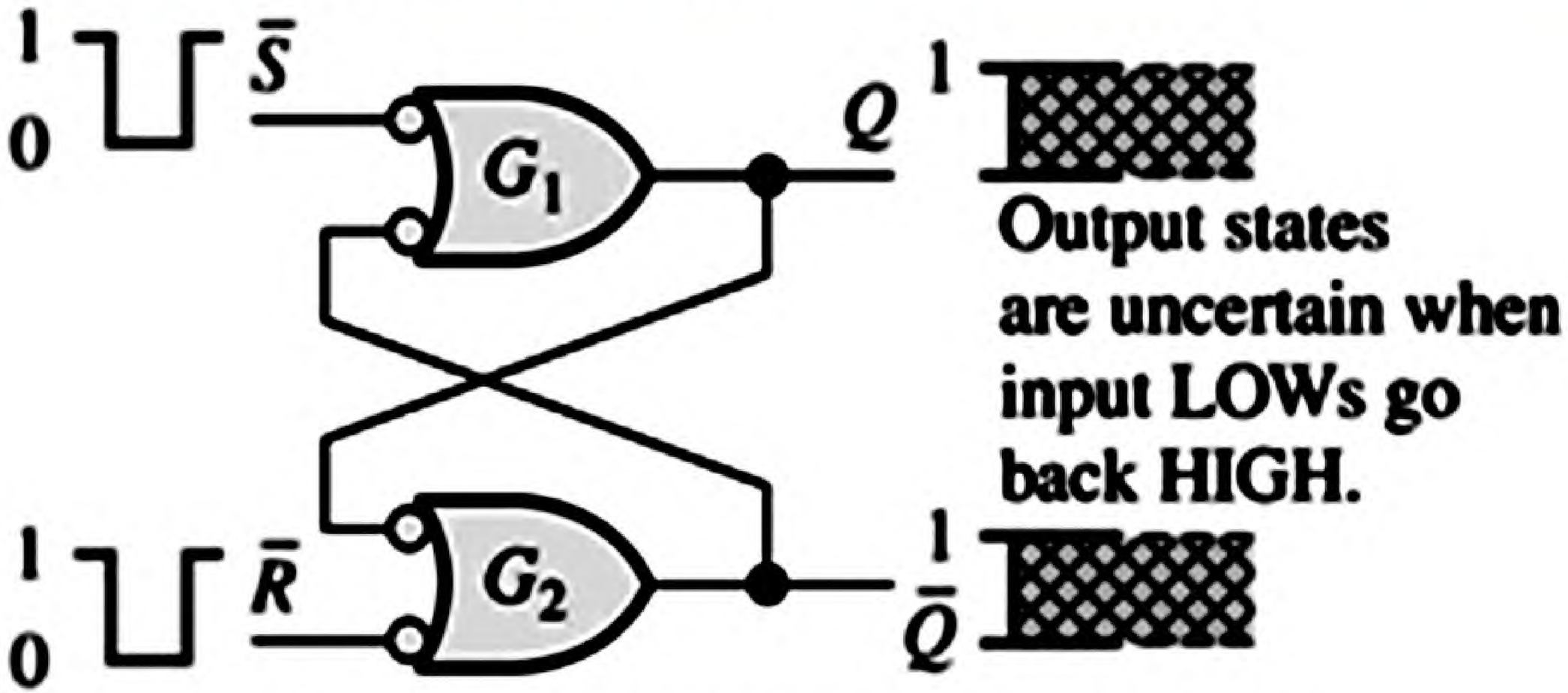


Latch starts out RESET ($Q = 0$).



Latch starts out SET ($Q = 1$).

- ✓ An **invalid condition** in the operation of an **active-LOW** input S-R latch occurs when **LOWs** are applied to **both** $\overline{S}$ and $\overline{R}$ at the **same time**.



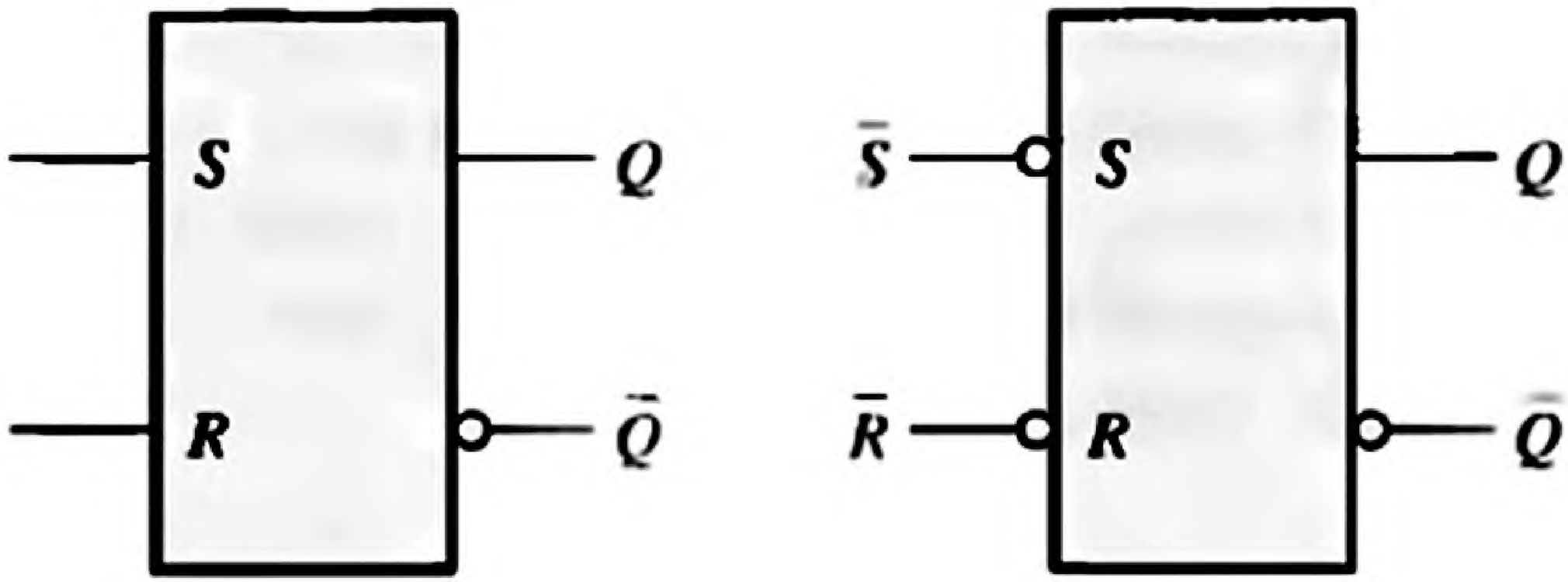
Simultaneous LOWs on both inputs

- ✓ As long as the LOW levels are simultaneously held on the inputs, both the Q and $\overline{Q}$ outputs are forced HIGH, thus violating the basic complementary operation of the outputs.
- ✓ Also, if the LOWs are released simultaneously, both outputs will attempt to go LOW.
- ✓ Since there is always some small difference in the propagation delay time of the gates, one of the gates will dominate in its transition to the LOW output state.

- ✓ This, in turn, forces the output of the slower gate to remain HIGH.
- ✓ In this situation, you cannot reliably predict the next state of the latch.

Table (1.1) Truth table for an active-LOW input $\overline{S}$ $\overline{R}$ latch.

Inputs		Outputs		Comments
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
1	1	NC	NC	No Change.
0	1	1	0	Latch SET
1	0	0	1	Latch Reset
0	0	1	1	Invalid condition

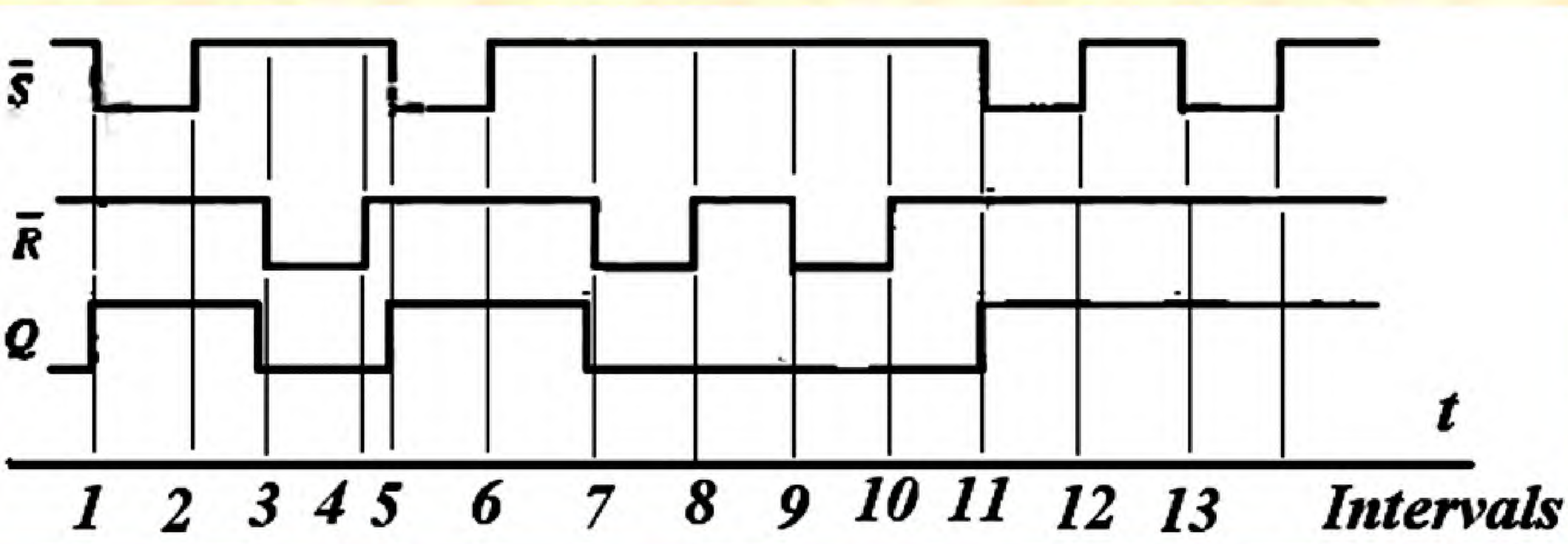


(a) Active-HIGH input S-R latch

(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

Figure (1.4) Logic symbols for the S-R and $\bar{S}$ - $\bar{R}$ latch.

Example (1.1): If the S and R waveforms in the Figure are applied to the inputs of the $\overline{S}$-$\overline{R}$ latch, determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.



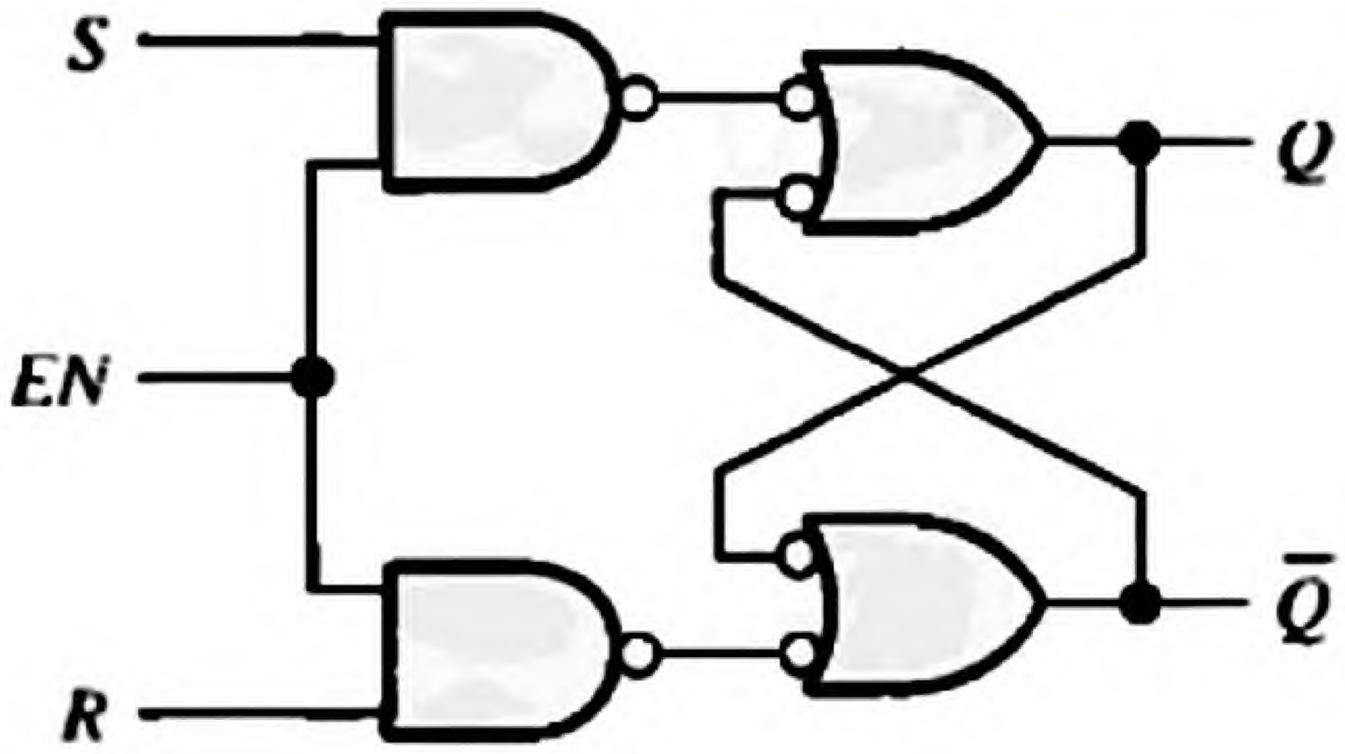
State Table

Interval	$\overline{S}$	$\overline{R}$	State	Q
0	1	1	Old value, NC	0
1	0	1	Set	1
2	1	1	NC	1
3	1	0	Reset	0
4	1	1	NC	0
5	0	1	Set	1
6	1	1	NC	1

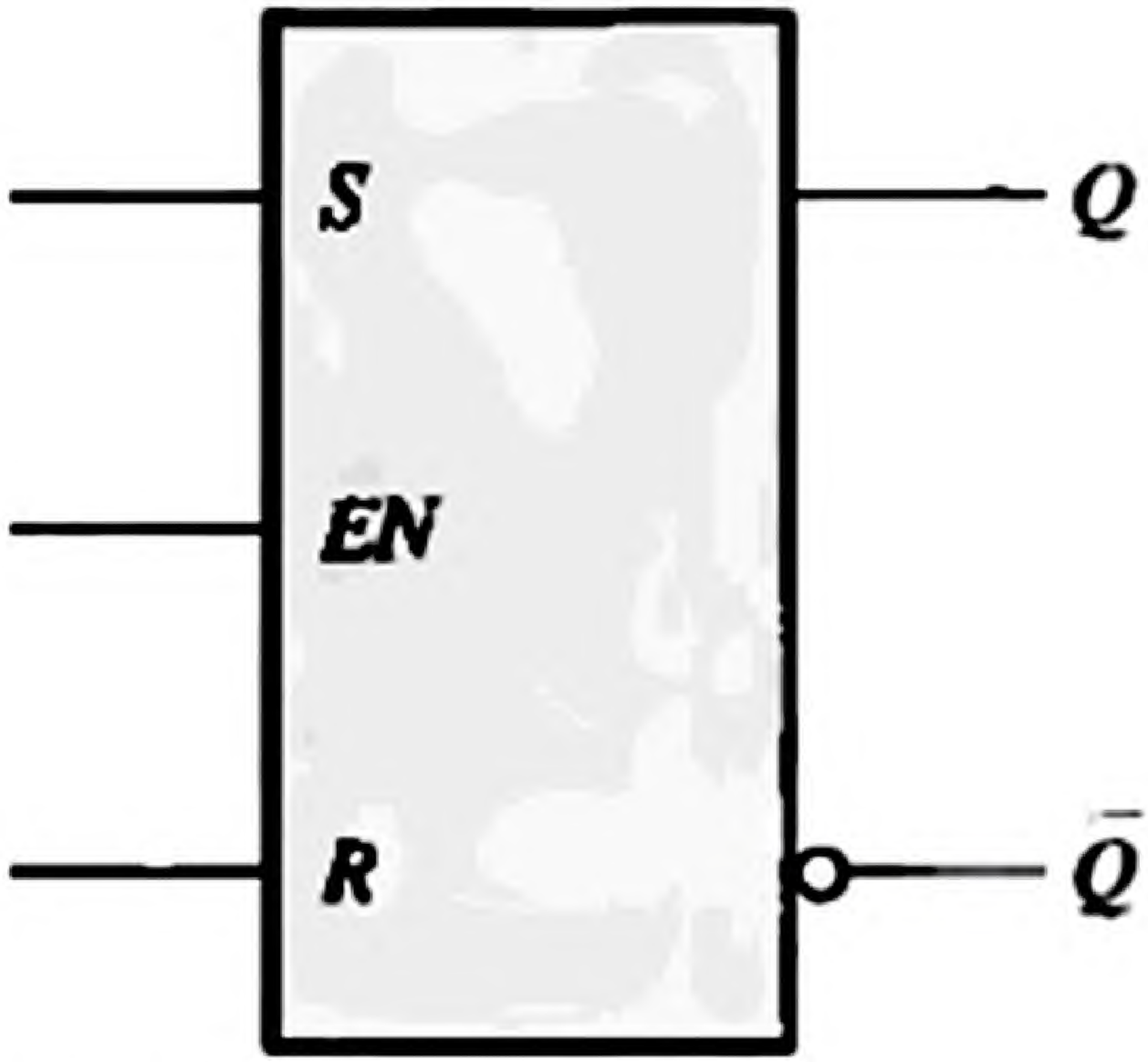
6	1	1	NC	1
7	1	0	Reset	0
8	1	1	NC	0
9	1	0	Reset	0
10	1	1	NC	0
11	0	1	Set	1
12	1	1	NC	1
13	0	1	Set	1
14	1	1	NC	1

1.3- The Gated S-R Latch.

✓ A gated latch requires an enable input, EN (G is also used to designate an enable input). The logic diagram and logic symbol for a gated S-R latch are shown in Figure (1.5).



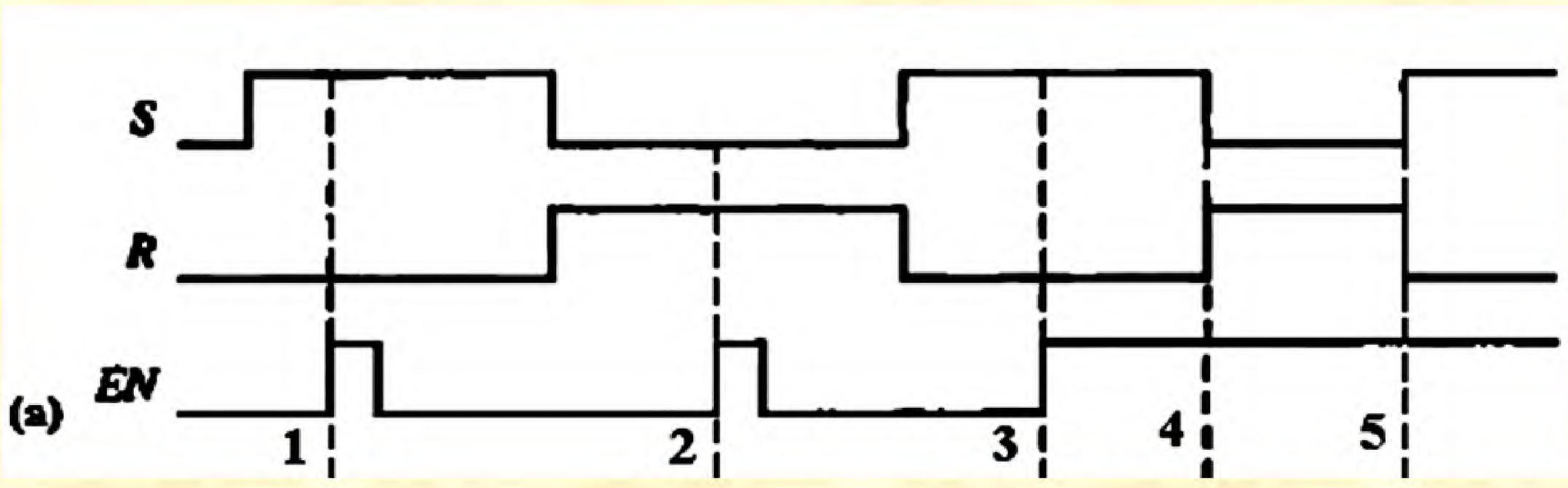
(a) Logic diagram



(b) Logic symbol

- ✓ The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input.
- ✓ The latch will not change until EN is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs.
- ✓ In this circuit, the invalid state occurs when both S and R are simultaneously HIGH.

Example (1.2): Determine the Q output waveform if the inputs shown in the Figure are applied to a gated S-R latch that is initially RESET.



State Table

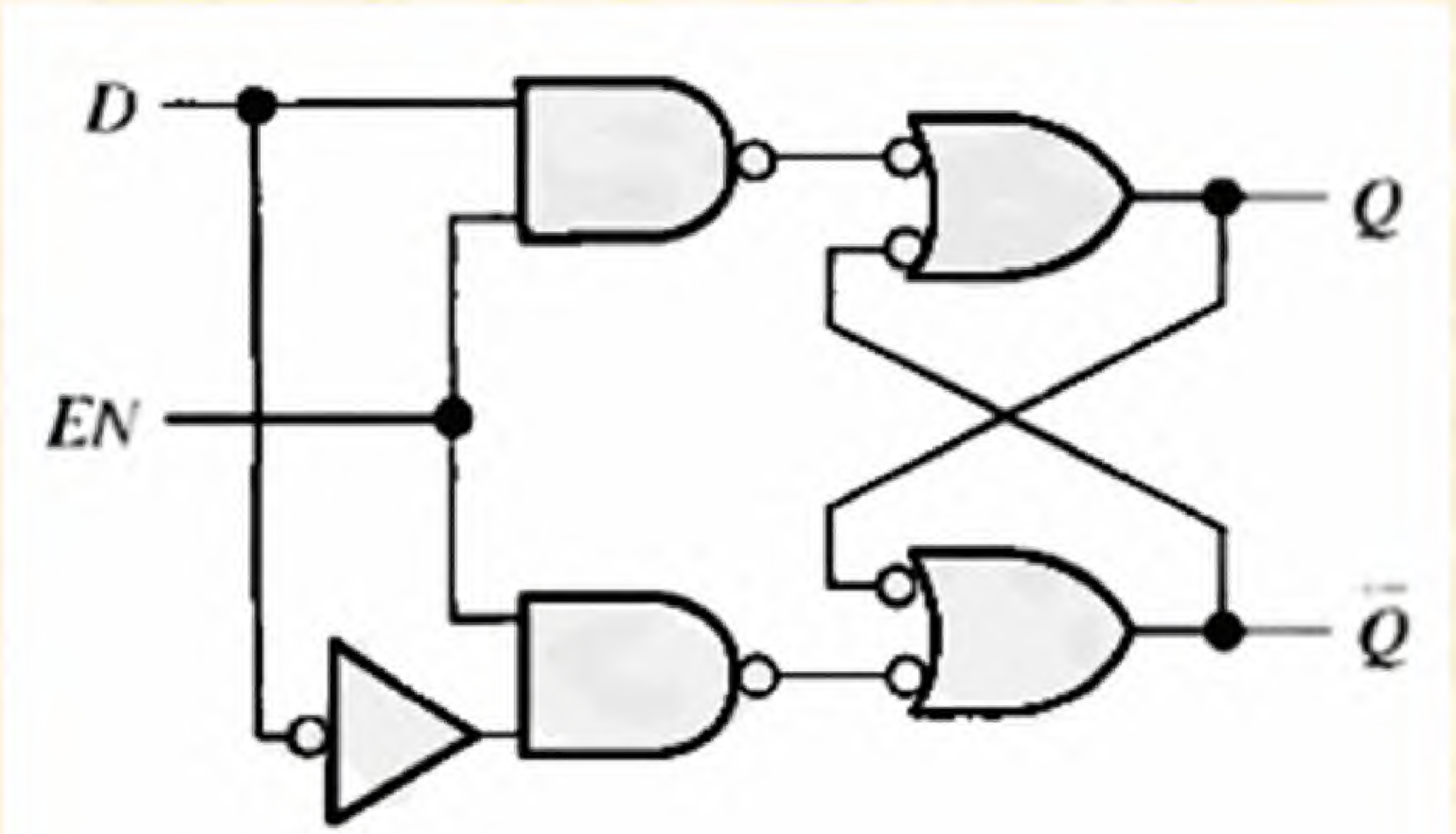
EN	S	R	State	Q
EN0	X	X	Old	0
EN1	1	0	Set	1
EN2	0	1	Reset	0
EN3	1	0	Set	1
EN4	0	1	Reset	0
EN5	1	0	Set	1

- ✓ When S is HIGH and R is LOW, a HIGH on the EN input sets the latch.
- ✓ When S is LOW and R is HIGH, a HIGH on the EN input resets the latch.

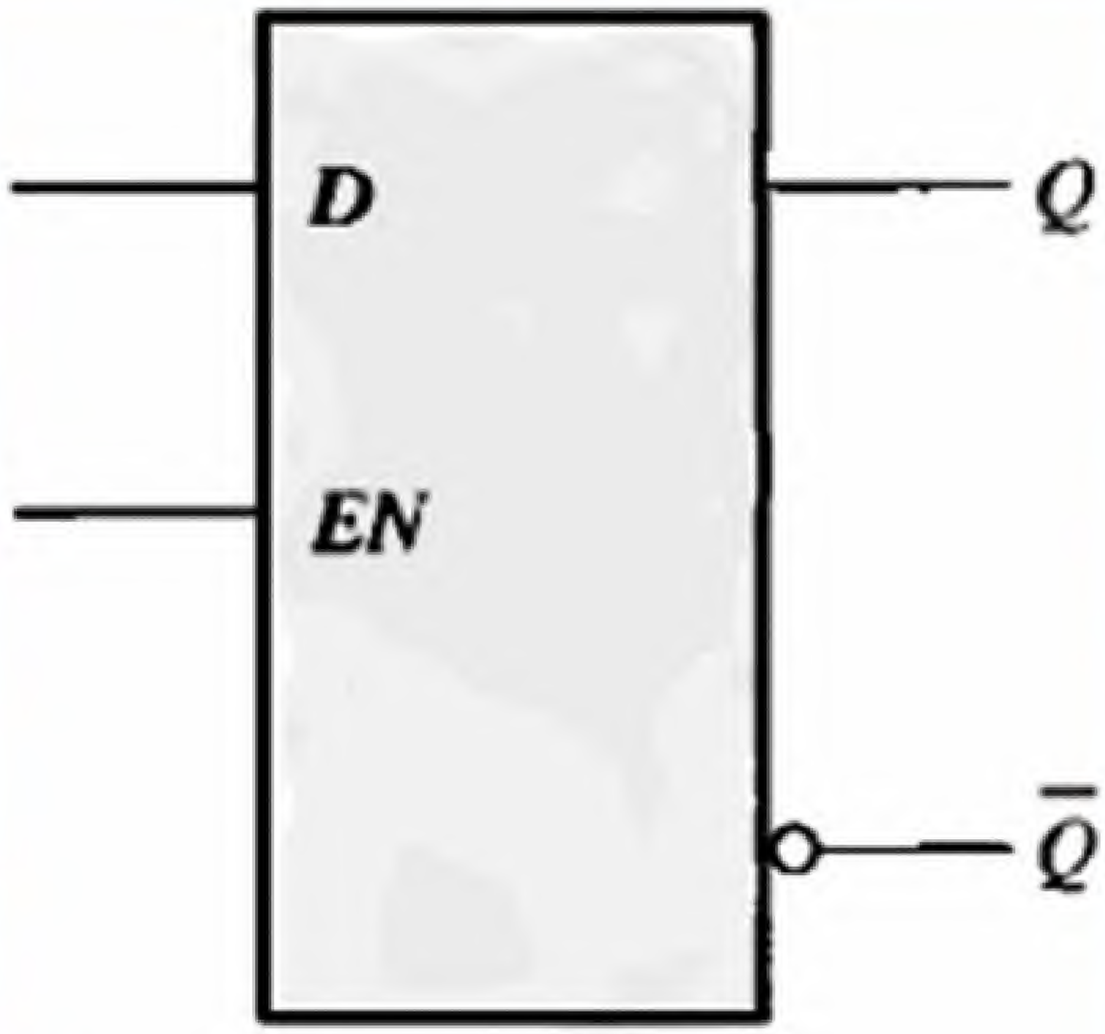
1.4- The Gated D Latch.

- ✓ Another type of gated latch is called the D latch.
- ✓ It differs from the S-R latch because it has only one input in addition to EN. This input is called the D (data) input.

✓ **Figure (1.6) contains a logic diagram and logic symbol of a D latch.**



(a) Logic diagram

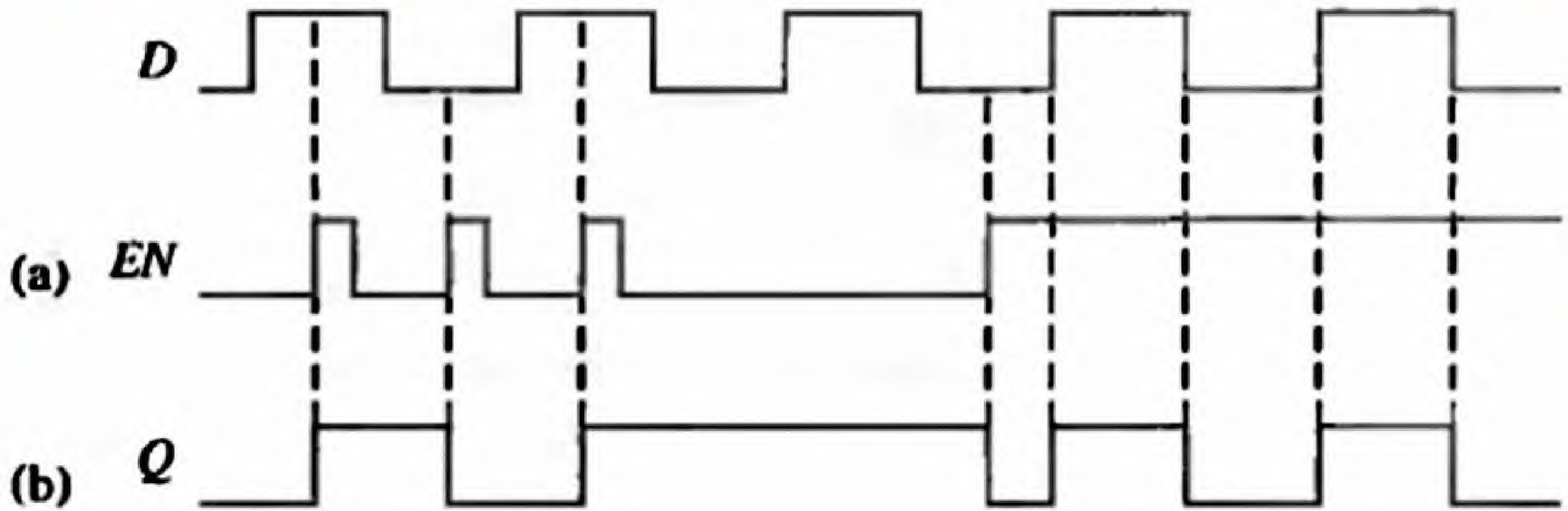


(b) Logic symbol

Figure (1.6) A gated D latch

- ✓ When the D input is HIGH and the EN input is HIGH, the latch will Set.
- ✓ When the D input is LOW and EN is HIGH, the latch will Reset.
- ✓ Stated another way, the output Q follows the input D when EN is HIGH.

Example (1.3): Determine the Q output waveform if the inputs shown in the Figure are applied to a gated D latch. which is initially RESET.

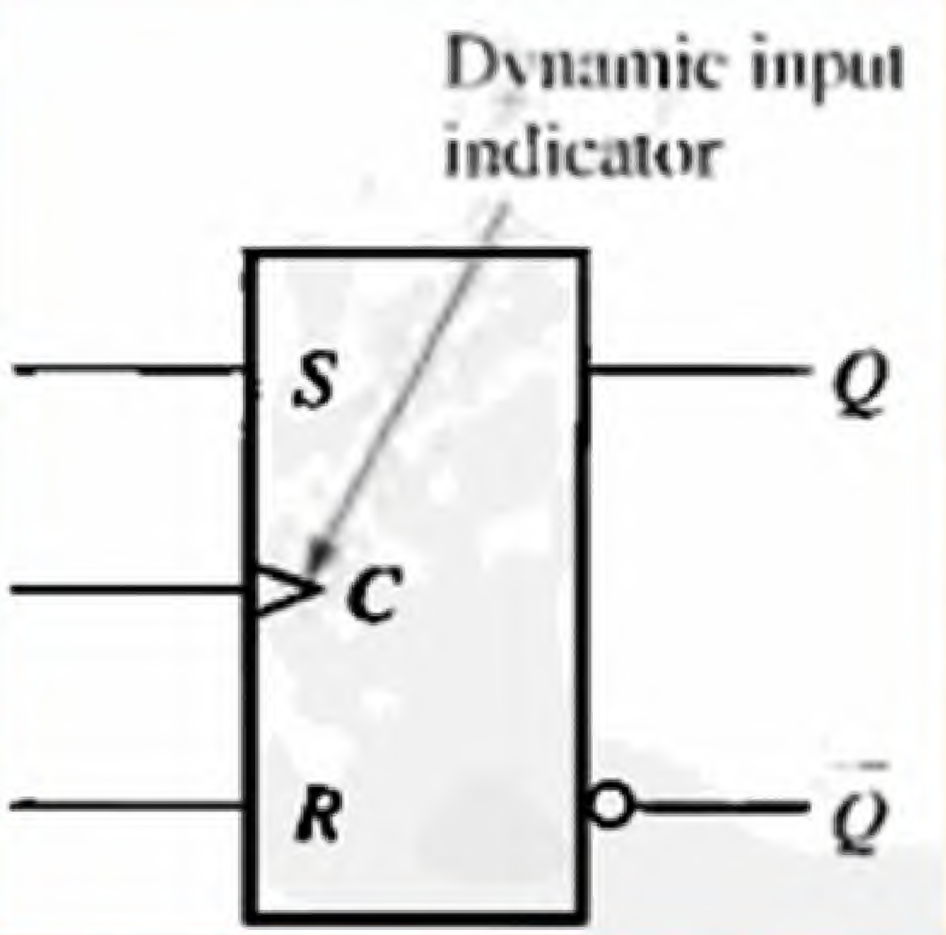


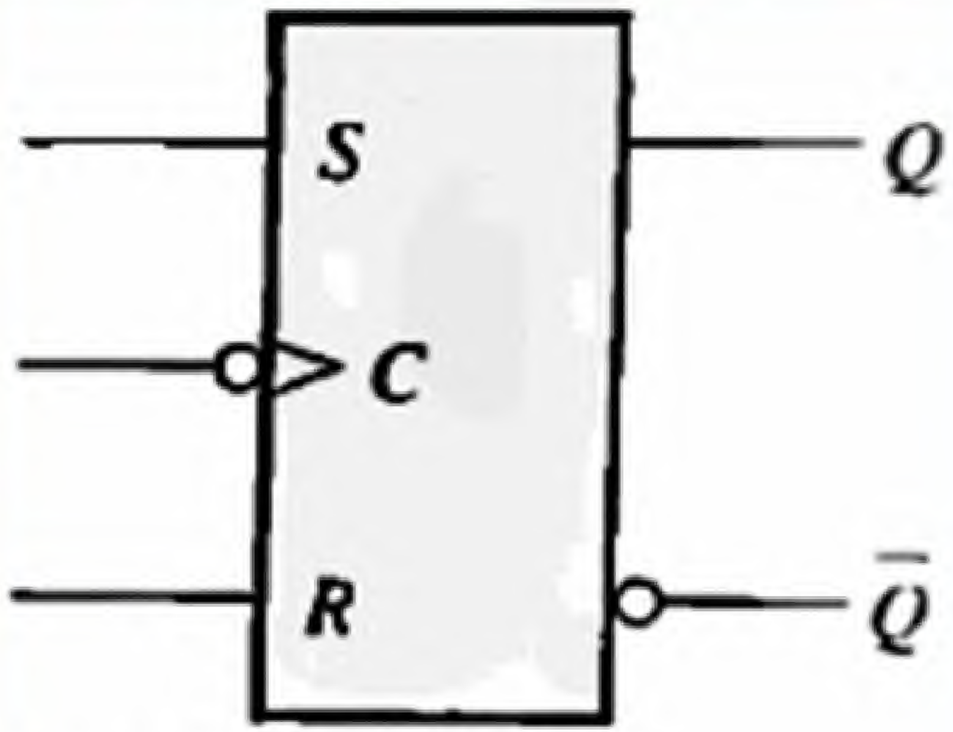
- ✓ When D is HIGH and EN is HIGH,. Q goes HIGH.
- ✓ When D is LOW and EN is HIGH, Q goes LOW.
- ✓ When EN is LOW, the state of the latch is not affected by the D input.

1.5-Edge Triggered Flip-Flop.

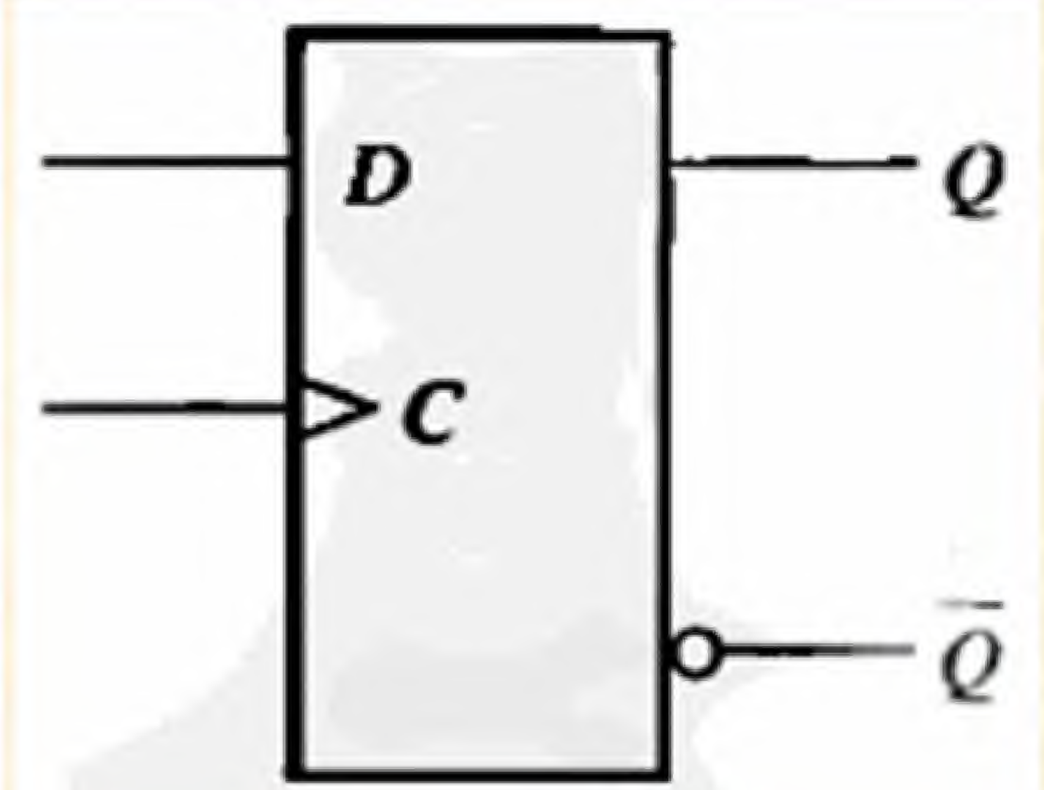
- ✓ An edge-triggered flip-flop changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.
- ✓ Three types of edge-triggered flip-flops are covered in this section: S-R, D, and J-K.
- ✓ Although the S-R flip-flop is not available in IC form, it is the basis for the D and J-K flip-flops.
- ✓ The logic symbols for all of these flip-flops are shown in Figure (1.7).

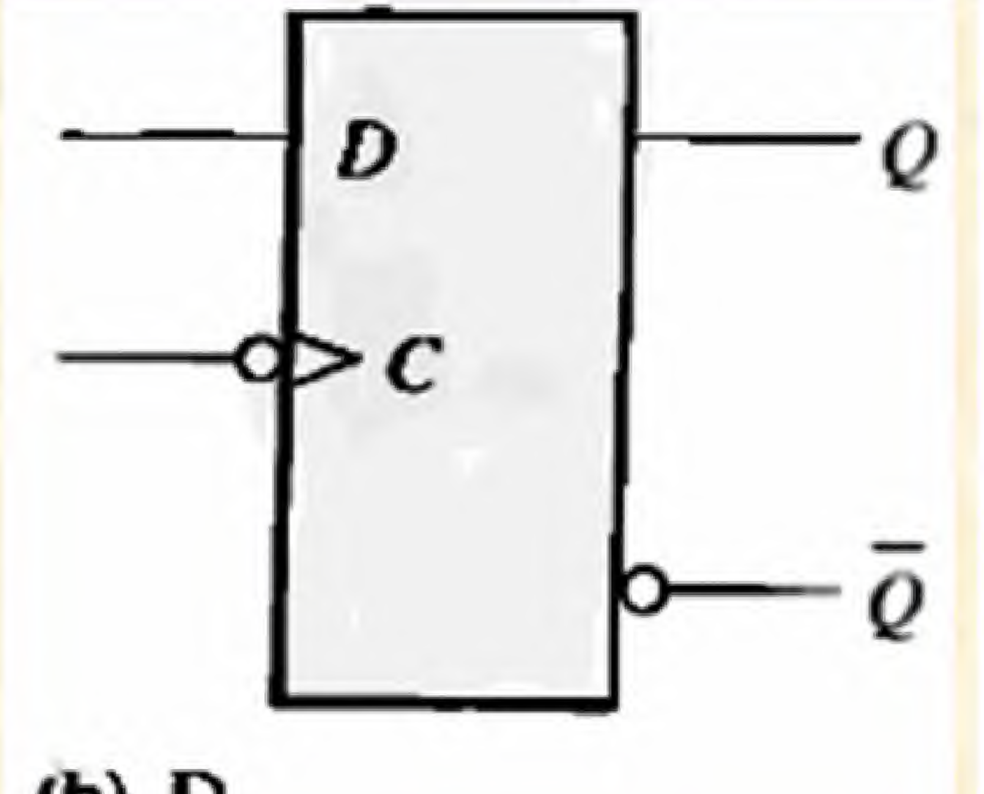
- ✓ Notice that each type can be either positive edge-triggered (no bubble at C input) or negative edge triggered (bubble at C input).
- ✓ The key to identifying an edge triggered flip-flop by its logic symbol is the small triangle inside the block at the clock (C) input.
- ✓ This triangle is called the dynamic input indicator.



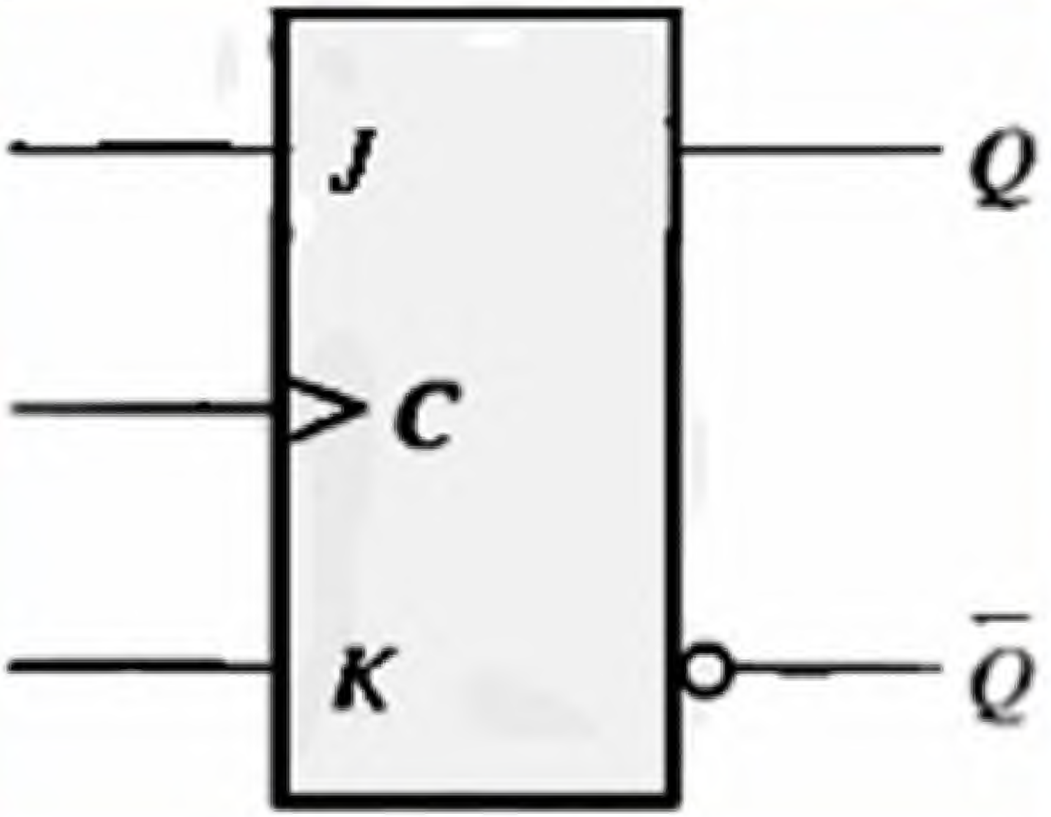


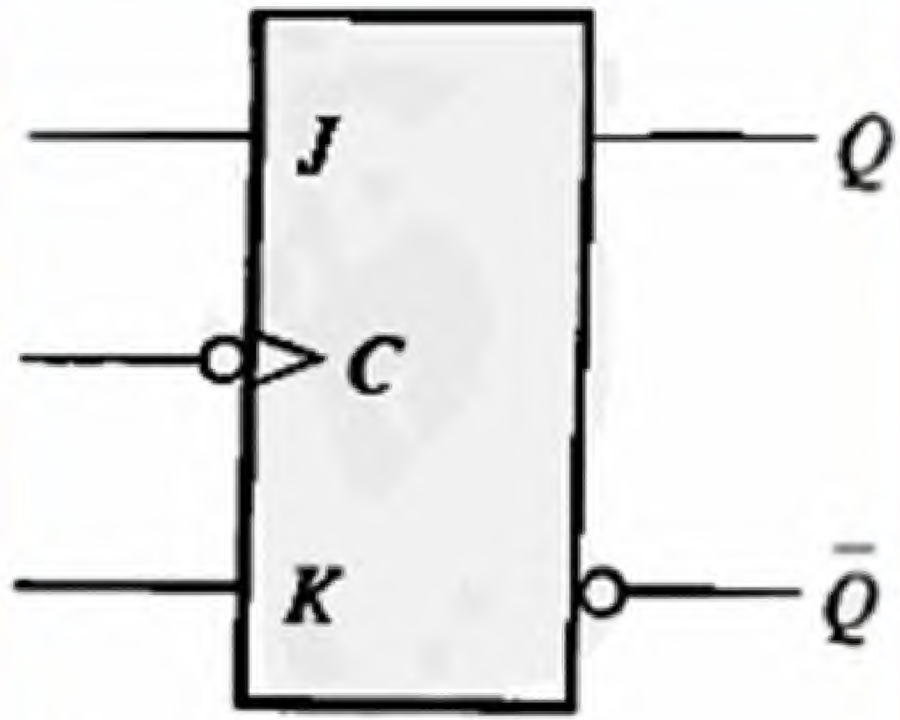
(a) S-R





(b) D





(c) J-K